# TRANSFERRED ELECTRON LOGIC DEVICES (TELDs) FOR GIGABIT RATE SIGNAL PROCESSING*

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## Abstract

Planar GaAs transferred-electron logic devices (TELDs) have been fabricated and their performance studied. The devices are evaluated as threshold logic elements. The parameters studied are (1) switching characteristics, (2) shortest pulses that can be processed, and (3) device delay and dissipation. Pulses as small as 80 ps wide can be processed through transferred electron logic gates (TELGs) with device delays of the order of 50 ps and delay dissipation product of 5-10 pJ which makes it suitable for gigabit rate signal processing.

## Introduction

Sugeta et al.[1] showed that Schottky barrier gate transferred electron devices can provide (a) small delay, (b) small delay-dissipation product, (c) input-output isolation, and (d) fan-out. These properties make the transferred electron logic device a good choice for gigabit rate signal processing. In view of this, both theoretical and experimental investigations have been carried out on TELDs. Hartnagel[2] found that the ratio of the load resistance ($R_L$) to device low field resistance ($R_o$) should be about 1-2 to develop a sizeable voltage in TELGs. Mause et al.[3] pointed out that the external charging time constant ($R_LC$) will limit the device performance rather than the domain formation times. Upadhyayula[4] studied the effect of the load resistor and the low field transconductance ($g_m$) of the device on the trigger sensitivity and showed that good low field $g_m$ is required for better device performance. Planar GaAs TELDs have been fabricated using these guidelines. The devices have been evaluated and the results are presented below.

## Device Fabrication

Thin GaAs wafers epitaxially grown using RCA's vapor hydride synthesis technique[5] on semi-insulating substrates have been used for device fabrication. The doping density and thickness of the active layer are $1\text{-}4\times10^{16}$ $cm^{-3}$ and 3-4 μm, respectively. The device geometry has been defined by standard photolithographic techniques. Evaporated Au:Ge/Ni:Au was used to obtain good ohmic contacts and evaporated Cr/Au was used for Schottky barrier gates. Fig. 1 shows a typical fabricated device. The cathode-anode spacing is 12 μm, cathode-gate spacing is 1-2 μm, gate length is 2 μm, and width is about 120 μm. The device low field resistance is 30-70 Ω and threshold current ≈ 50 mA.

## Device Evaluation

The TELDs have been evaluated as threshold logic elements. Fig. 2 shows the switching characteristics of a TELD. A 100-Ω anode load resistor ($R_L/R_o \simeq 1.5$) was used. The output of the gate was below 0.2 V for input signals less than 1.15 V and above 1.2 V for input signals greater than 1.2 V. The switching transition occurs within 50-70 mV. Device delay (which is the time elapsed before the output is produced after an input signal is applied) on a similar device has been measured on a sampling oscilloscope. The electrical paths in both the reference (input) and test (output) channels were made equal. Fig. 3 is a sampling scope waveform of the input and output signals. The propagation delay for this particular device is less than 50 ps and the delay-dissipation product is 10 pJ. The smallest device delay measured was 20 ps and delay-dissipation was 2.3 pJ. In order to verify that the output of a transferred electron logic gate is large enough to trigger a similar gate, a two-gate cascaded circuit was studied. A cathode load resistor was used in the first gate to provide an output pulse of the same polarity as the input pulse. Anode load resistor was used for the second gate. A step recovery diode pulse shaping circuit was used to sharpen the output pulse from a charge-line-pulser. An output pulse less than 160 ps at the maximum height was used as a test pulse. Fig. 4 shows the response of the two logic gates for an input pulse above the threshold value for TELG-1. The output pulses from the transferred electron logic gates are less than 100 ps at half height and correspond to single domain transit time in both these devices. Near transit time oscillations were observed when wide input test pulses were used.

A two-input AND gate was also evaluated to show the potential of TELDs. The output of two TELGs were summed in a resistive summing network and the output of the summing network was fed to a third TELD. The summing network and the threshold gate form the AND circuit. A charge-line-pulser and a resistive divider network provided the input pulses to the two threshold gates. The electrical paths of these two pulses were made equal. Figs. 5 and 6 show the performance of the AND gate. The output of one of the threshold gates is also included here. The AND gate output is present only when both the threshold gates are triggered, as it should. Input pulse width less than 500 ps was used in testing this circuit. A double pulse with about 800 ps separation between the two pulses was also processed through this circuit successfully. This puts the resolution of the circuit to be better than 800 ps. This value of 800 ps pulse separation is the limit of our test equipment but definitely not the resolution limit of the TELD circuit.

## Conclusions

Transferred electron logic devices have been fabricated and evaluated as threshold logic elements. Pulses as small as 80 ps were processed and device delays of the order of 50 ps were measured. The suitability of these devices for gigabit rate signal processing has been demonstrated.

## References

1. T. Sugeta et al., "Characteristics and Applications of a Schottky-Barrier-Gate Gunn-Effect Digital Device," IEEE Trans. Electron Devices, Vol. ED-21, pp. 504-515, Aug. 1974.

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2. H. L. Hartnagel, "Theory of Gunn-Effect Logic," Solid State Electronics, Vol. 12, pp. 19-30, Jan. 1969.

3. K. Mause, A. Schlachetzki, E. Hesse and H. Salow, "Monolithic Integration of Gallium Arsenide-Gunn Devices for Digital Circuits," Proc. Fourth Biennial Cornell Electrical Engineering Conf. on Microwave Devices, Circuits and Applications, Vol. 4, p. 211, 1973.

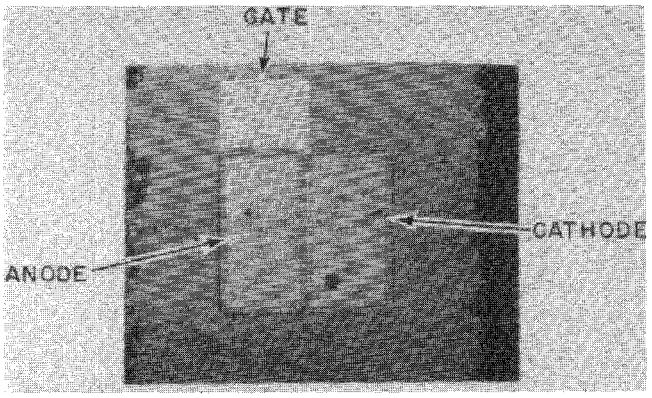


Figure 1. Multi-level mesa type TELD. $\ell_{ca}$=12μ, $\ell_g$=2μ, $\ell_{cg}$≃1-2μ and W (average) = 150μ.

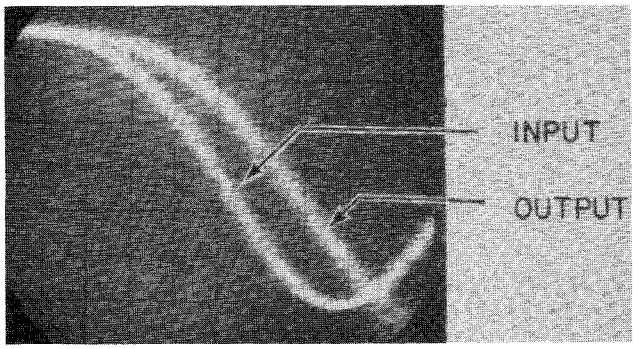


Figure 2. Input-output characteristic of TELD.

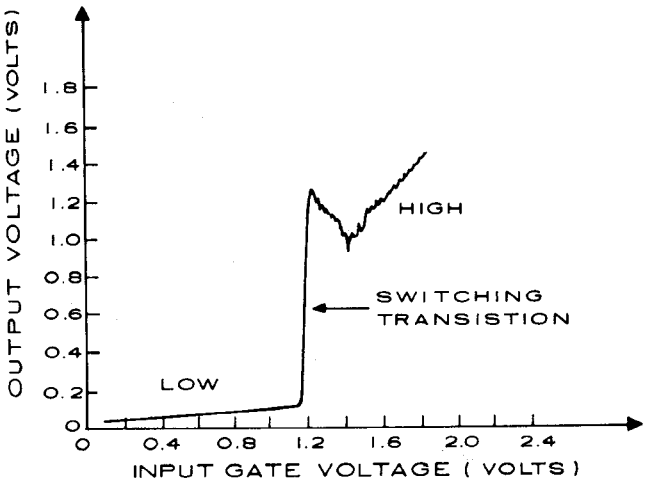


Figure 3. Photograph of sampling oscilloscope waveforms of the input and output signals showing the device delay in a planar TELD.

4. L. C. Upadhyayula, "Trigger Sensitivity of Transferred Electron Logic Devices (TELDs)," to be published in IEEE Trans. Elec. Devices.

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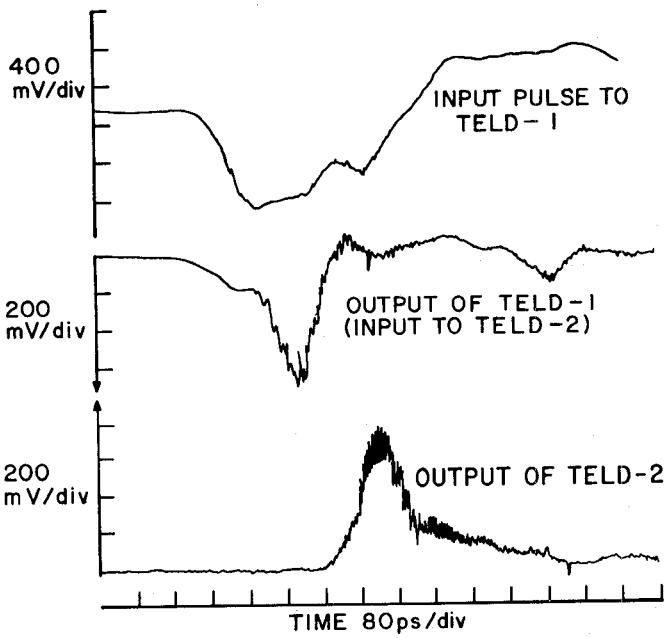


Figure 4. Response of a cascaded TELD circuit for input signal above threshold.

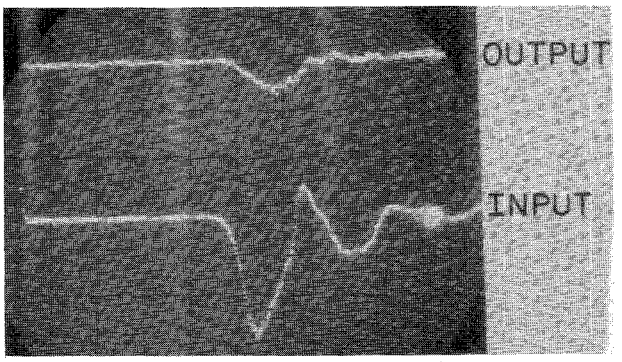


Figure 5. Performance of a TELD-AND circuit when only one input is present. Top trace: output- 100 mV/div; bottom trace: input - 180 mV/div; horizontal scale: 500 ps/div.

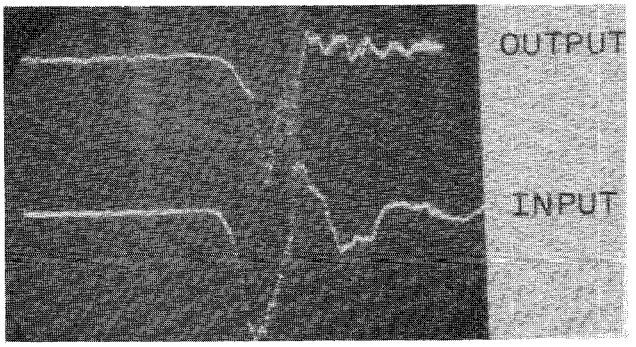


Figure 6. Performance of a TELD-AND circuit when both the inputs are present. Top trace: output-100 mV/div; bottom trace: input-180 mV/div.